

POWER TO THE DSP

New Torex DC-DC converter is ideal for telecoms designs

Digital Signal Processors (DSPs) are having a major impact on telecoms equipment design. The processing power of the latest generation DSPs is not only allowing existing services to handle more calls in less space but it is also enabling designers to realise new systems and services, such as voice over IP, which until now were out of reach. The new DSPs employ the very latest low power CMOS technology operating at voltages between 1.5V and 1.8V, and demand a highly efficient power management technology to match. Torex Semiconductor's new XC9201/02 range of step down DC-DC converters has been developed to answer these demands.

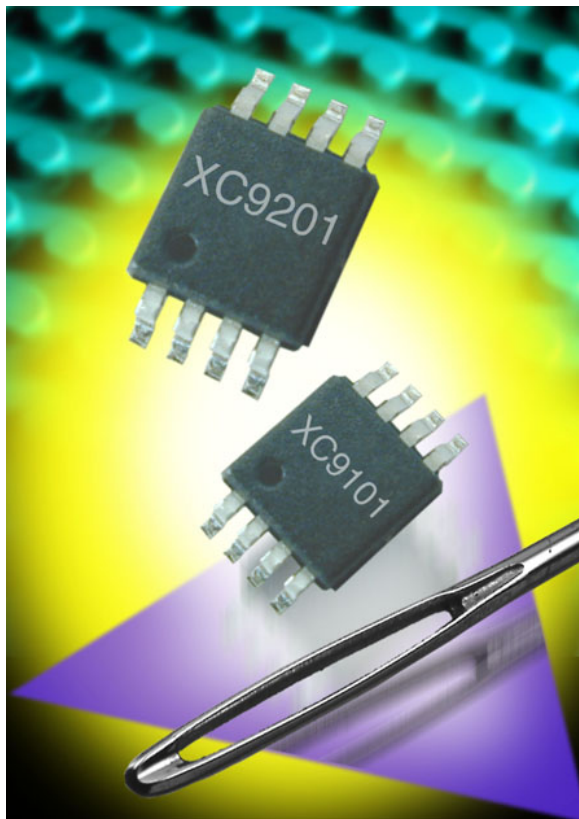


Figure 1 shows the internal layout of the new DC-DC converter controller ICs. Both the XC9201 and XC9202 employ pulse width modulation (PWM) for the multiple feedback signals of the output voltage and coil current. However, the XC9202 with PWM operation at moderate to high loads, has the facility to switch under low loading

to pulse frequency modulation (PFM), giving high efficiency and low ripple across a wide load range. With an input voltage range of 2.2V to 20V the controllers are available in pre-set output voltages (the C series), or with a wide range of externally selectable voltages from 1.2V to 16V (the D series). The output voltage is set simply by attaching externally dividing resistors.

Employing the very latest current/voltage multiple feedback technique means that ceramic capacitors can be used to stabilise the XC9201/02's output rather than the tantalums required by most DC-DC controller ICs. This brings significant savings in terms of both space and cost.

All internal sequencing is synchronised by the internal clock combined with a capacitor and a resistor to generate regular pulses with sawtooth waveforms. Any frequency can be selected from a wide range of 100kHz to 600kHz, simply by choosing the correct combination of capacitor and resistor attached to the CLK pin.

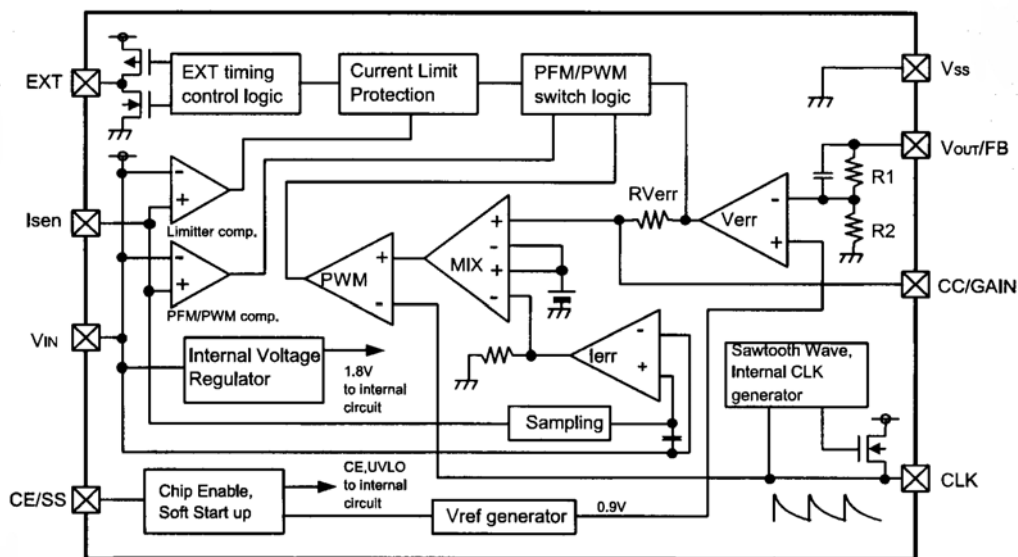


Fig.1: Internal layout of XC9201/02.

The Verr amplifier is designed to monitor the output voltage. In the case of the C type devices the pre-set voltage from resistors R1 and R2 are compared to a 0.9V reference voltage. For type D devices the externally selected voltage from the FB pin

is compared to the 0.9V reference. For all types of controller in response to a voltage lower than the reference voltage the amplifier responds by increasing the voltage output.

The Verr amplifier output goes to both the PFM/PWM logic switch and the mixer via a resistor (R_{verr}). The signal to the logic switch acts as the voltage sensor in PFM mode while the one to the mixer is the pulse width control signal in PWM mode. Gain and frequency characteristics of the Verr can be externally set.

The Ierr amplifier monitors the coil current. The potential difference between the V_{IN} and I_{SEN} pins are sampled each time there is a switching operation. Then the potential difference is amplified or held, as necessary, and input to the mixer. Next the Ierr outputs a signal ensuring that the greater the potential difference between the V_{IN} and I_{SEN} pins, the smaller the switching current. Its gain and frequency characteristics are fixed internally.

The mixer modulates the signal sent from the Verr amplifier with the signal from the Ierr amplifier. This modulated output signal then enters the PWM comparator for comparison with the sawtooth pulses generated at the CLK pin. If this signal is greater than the sawtooth waveforms, a signal is sent to the output circuit to turn on the external switch.

The current flowing through the coil is monitored by the limiter comparator via the V_{IN} and I_{SEN} pins. The limiter comparator outputs a signal when the potential difference between the V_{IN} and I_{SEN} pins reaches 150mV or more. This signal is converted to a logic signal and handled as a DFF reset signal for the internal circuit. When a reset signal is input, a signal is output immediately at the EXT pin to turn off the MOS switch. When the limiter comparator sends a signal to enable data acceptance, a signal to turn on the MOS switch is output at the next clock pulse. If at this time the potential difference between the V_{IN} and I_{SEN} pins is great, operation is repeated to turn off the MOS switch again. DFF operates in synchronisation with the clock signal on the CLK pin.

The soft start function is made available by attaching a capacitor and resistor to the CE/SS pin. The reference voltage applied to the Verr amplifier is restricted by the

start-up voltage of the CE/SS pin. Doing so ensures that the Verr amplifier operates with its two inputs in balance, thereby preventing the ON-TIME signal from becoming stronger than necessary. Consequently, soft start time needs to be sufficiently longer than the time set to CLK. The start-up time of the CE/SS pin equals the time set for soft start.

Undervoltage lock out (UVLO) is also provided. This function is activated to turn off the MOS switch attached to the EXT pin when the input voltage (V_{IN}) decreases to approximately 1.4V or below. The purpose of this function is to keep the external MOS switch from turning on when a voltage at which the IC operates unstably is applied. UVLO also restricts signals during soft start so that the external MOS switch does not turn on until the internal circuitry becomes stable.

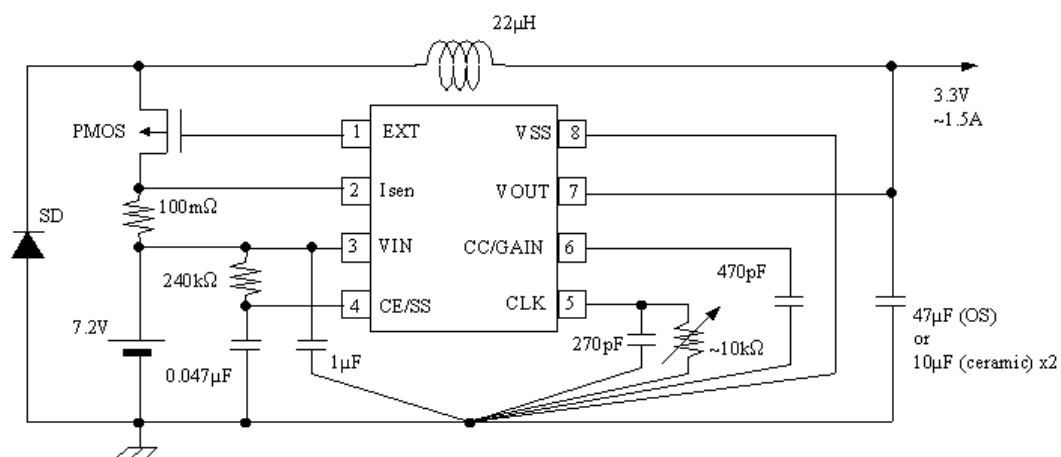


Fig.2: Typical application configuration.

Figure 2 shows a typical application configuration based on the 1.8V output part, the XC9201D09AKR. The PMOS transistor used in the circuit is a Torex XP132A11A1SR; the Schottky diode a Toshiba U3FWJ44N, and the 22μH coil, a Sumida CDRH127.

The high levels of efficiency achieved by the device at input voltages ranging from 2.5 to 5.0V are shown in Figure 3. As can be seen, even with an output current of only 10mA, the 1.8V output converter provides an acceptable level of performance.

Efficiency vs Output Current (Topr = 25°C)

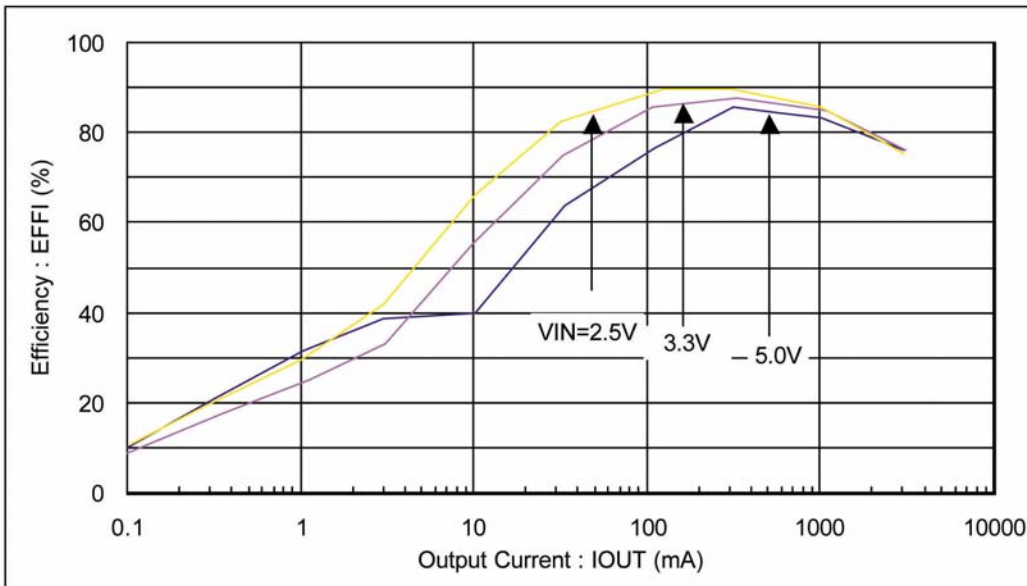


Fig.3: High levels of efficiency.

Output Voltage vs Output Current (Topr = 25°C)

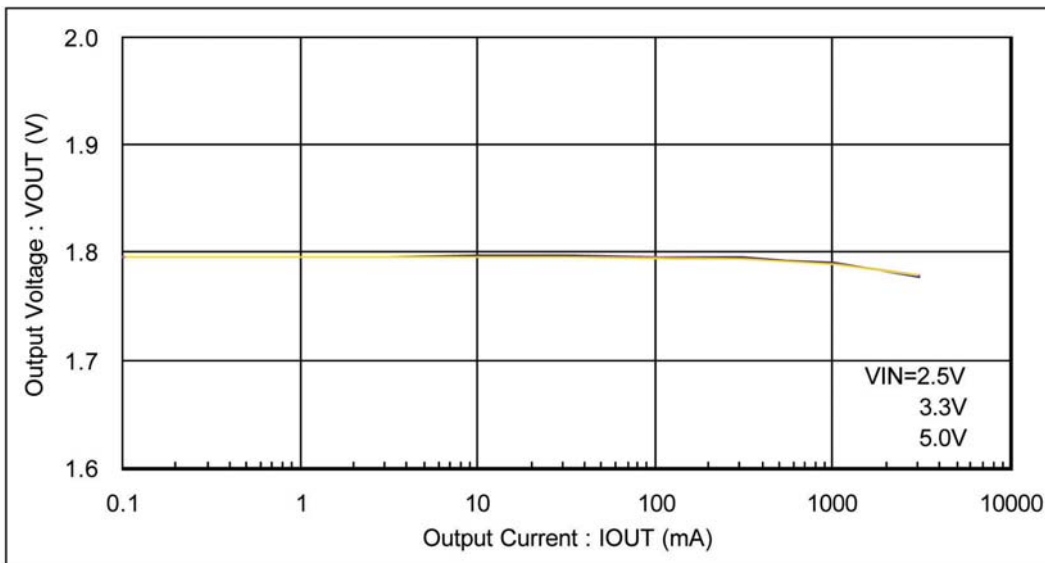


Fig.4: Voltage output remains constant.

Beyond 10mA significantly high levels of efficiency are achieved. The XC9201 has a highly stable output. Figure 4 shows that the device's voltage output remains constant over a very wide range of output currents. Figure 5 plots ripple against output current and highlights the device's low ripple across a wide load range.

The controllers of the XC9202 series switch between PFM and PWM modes automatically. The PFM/PWM comparator monitors the current each time switching occurs. When the current decreases to a certain value or below, a shift from PWM to PFM mode takes place.

Ripple Voltage vs Output Current (Topr = 25°C)

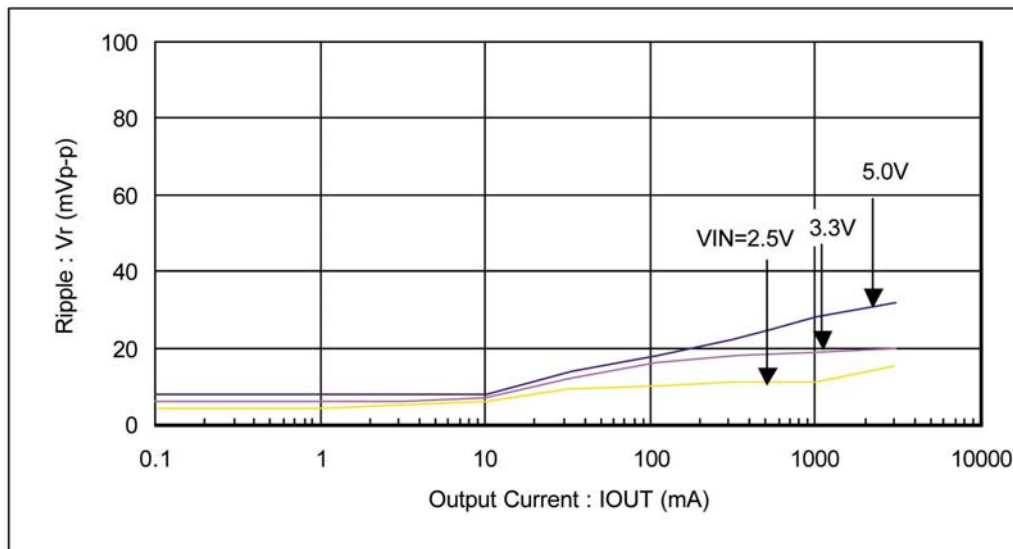


Fig.5: Low ripple across a wide load range.

When V_{OUT} (or the FB voltage in the case of the type D) decreases below the set value, the Verr amplifier sends a signal directly to the logic block to turn on the external MOS switch. An ON signal is output from the EXT pin in synchronisation with the clock signal of the CLK pin. When the external MOS switch is turned on a current flows through the coil at the same time. The external MOS switch is turned off by: a current-limit signal of the limiter comparator (set to a different level than the limiter voltage in PWM mode), the leading edge of the next clock signal or an increase in the output voltage. The logic is programmed for the PFM mode so that a signal is generated in synchronisation with the leading edge of the clock signal at the CLK to turn off the external switch for a fixed period.

The controller stops required operation if the output voltage exceeds the set value after a single cycle of switching operation and waits for another drop in the output voltage. If the set value is not exceeded pulses are output successively. Since the

current flowing through the coil is limited by the limiter comparator, output voltage ripple is held below a certain value.

If the PFM/PWM comparator indicates PWM mode constantly as a result of frequent occurrence of successive pulses, the controller operates in PWM mode continuously. As the PWM mode is active constantly behind the PFM mode, shifting between modes happens smoothly. Clock pulses at the CLK pin do not stop even in PFM mode.

The high level of flexibility inherent in the new XC9201/02 allows designers to tailor its operation to closely match the parameters of their own particular applications. Telecoms designers looking to power the latest DSPs in their next generation equipment designs should look no further than this incredibly efficient low cost power management solution.