

PLL CLOCK GENERATOR IC - A CLEAR ALTERNATIVE TO CONVENTIONAL CRYSTAL OSCILLATORS

Within electronic designs, the 'traditional' and most common way of generating clock signals for ICs of ever-increasing complexity is via a crystal oscillator. Crystal oscillators, however, are not cheap and can be a major cost burden particularly in portable and hand-held designs. Fear not - Torex Semiconductor has developed a cheaper alternative - the new XC25BS3 series of high frequency PLL clock generator ICs, with built-in divider and multiplier circuits.



The new PLL clock generator IC makes use of external clock signals that are to be found in most electronic systems, from the counter of a CPU for example. Using this low frequency (a few tens of kHz) clock signal as input, the XC25BS3 is able to output a clock signal of a few tens of MHz that can then be used as the main clock signal to another chip. The output frequency is a multiplication factor of the input and

in sync with it. Input frequencies can be from 14kHz to 35MHz. Also, by using a program on the CPU side of the circuit to change the supplied clock input, it is possible to vary the output clock frequency of the XC25BS3.

Employing low power CMOS technology, the new XC25BS3 series combines crystal oscillator circuits, divider circuits and multiplier PLL circuits in a single chip. Its SOT-26 package contains several blocks including: 11-step input counter, 11-step feedback counter, VCO and LPF (Fig. 1).

The XC25BS3's inherent flexibility lies in its two outputs. The first, Q_0 , is equal to the product of the reference oscillation and the chosen multiplier/divider ratio within a frequency range of 9MHz to 80MHz. The second output, Q_1 , is a tri-state output selectable from reference oscillation, PLL frequencies/2, comparative frequencies/2 or GND. Output comparative frequencies are selectable within a 14kHz to 500kHz range.

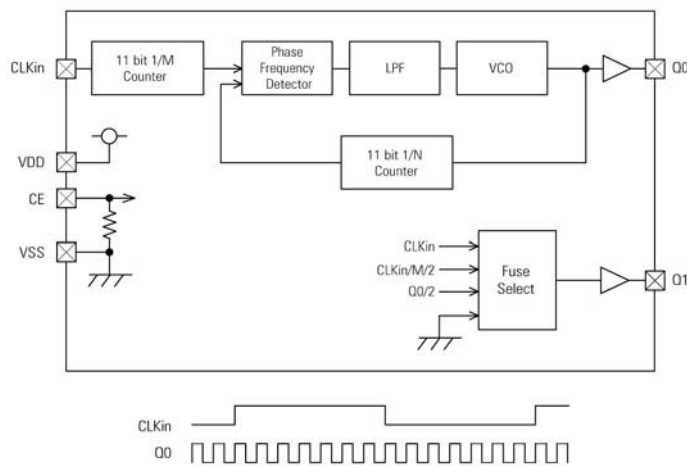


Fig.1: The XC25BS3 combines crystal oscillator, divider and multiplier PLL in a single chip.

Using laser trimming, the clock generator's frequency multiplication factor is factory set to a designated value. In addition to this, the whole loop plus LPF is trimmed to an optimum constant, matching the designated input and output frequencies. A

significant result of this trimming is an output clock signal of extremely small jitter, for example 30ps at an output frequency of 80MHz (Fig 2.).

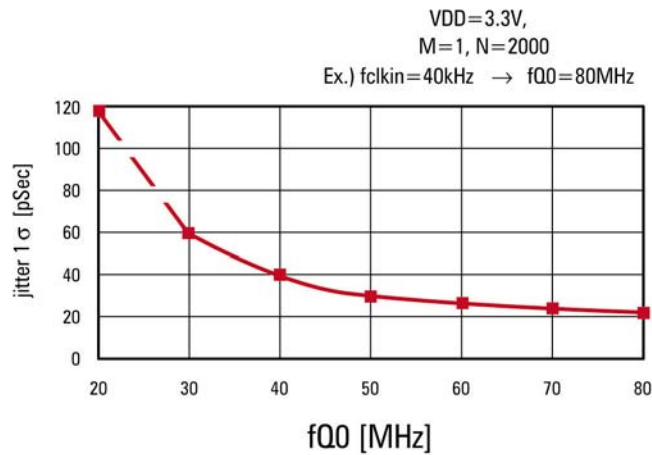


Fig.2: Output clock signals have extremely small jitter.

As an example, suppose a clock signal output of 36.864 MHz is required from an input clock signal, *fclkin*, of 27MHz. By trimming the IC to set the frequency division factor for the input counter, *M*, to 375 and the frequency division factor for the feedback counter, *N*, to 512, it is possible to gain the desired output frequency, *Q₀*:

$$fclkin \times N/M = 27\text{MHz} \times 512/375 = 36.864 \text{ MHz}$$

M, for the input counter, can be selected within a range of 1 to 2047, and *N*, for the feedback counter within a range of 20 to 2047. Accordingly, it is possible to choose virtually any frequency multiplication factor within the available input and output frequency ranges, with *N/M* not necessarily set as an integer.

The clock generator IC is able to make use of a wide variety of external clock signals, within a frequency range of a half to twice the device's designated frequency. The output frequency changes according to the input frequency. This means that a very wide spectrum of applications get optimum benefit of the PLL. The clock signal from the counter of a CPU is an excellent example of a common low frequency input. The XC25BS3 is able to take the few tens of kHz input from the counter and create an

output clock signal of a few tens of MHz that can then be used as the main clock signal to another chip (Fig. 3).

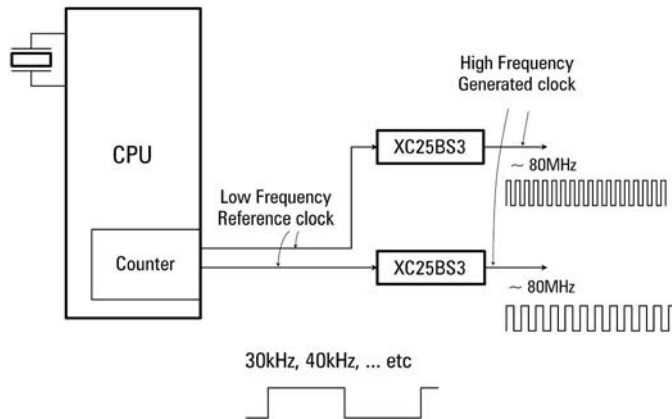


Fig.3: The XC25BS3 can be used to generate the main clock signal for another chip.

The device incorporates a CE function enabling designers to reduce current consumption down to 5 μ A (max.) in standby mode. Output Q₀ of the XC25BS3 can be set to a high impedance status using the CE pin. This makes it possible to change the main clock frequency supplied to another chip by controlling the CE signal with the output configured as wired or using two or more XC25BS3 ICs.

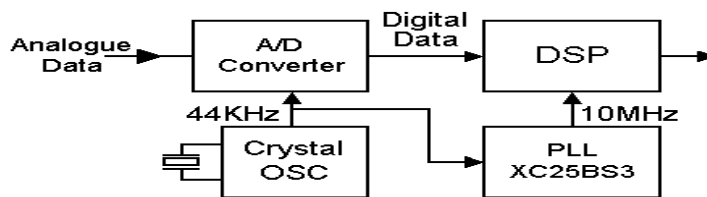


Fig.4: Built-in PLL overcomes synchronisation problems.

Now consider the case of sending and receiving data. The simplest method for data exchange is to synchronise it with a CLK control signal. However, there are

occasions when a synchronous clock signal cannot be obtained and thus synchronisation cannot be achieved, such as with radio frequencies where the receiver must synchronise the frequency to the transmitter's frequency.

A PLL built into the section of the application that controls the synchronisation of the transmission and receiving signals overcomes this problem (Fig 4). If the DSP's signal processing clock and the A/D converter's sampling time can be synchronised, data loss can be eradicated without having to raise the DSP's frequency above that which is necessary.

There are other cases where it is desirable to have a clock signal in synchronisation with a reference frequency. As Fig 5 illustrates, even using two systems employing the same 10MHz crystal, oscillation frequencies will show slight differences when measured. This is because the CLK output of CPU board 1 and CPU board 2 are not synchronous. However, with the addition of a PLL like the XC25BS3, two synchronous clock outputs can be achieved.

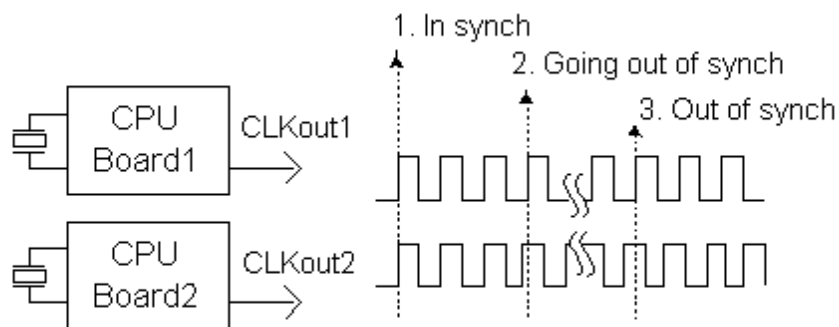


Fig.5: Slight differences in oscillation frequency will occur even when using the same 10MHz crystal.

In Fig 6, a 30MHz crystal oscillator (CLKout1) is divided by 3 to produce a 10MHz (CLKout2) signal. By using this signal and multiplying it by 3 by means of a PLL (XC25BS3), a 30MHz output is achieved (CLKout3). The PLL operates in

synchronisation with the rising edge of CLKout2. In the case of the timing in '1', the 'out3' signal is slightly behind that of 'out2' and so the oscillation frequency will increase so that by '2', the phase is in synch. However, as the frequency is now too fast, by '3' the signal at 'out3' is ahead of that at 'out2'. In order to correct this disparity, the frequency is this time reduced. By '4' the signal 'out3' is once more behind that of 'out2' and so the cycle continues.

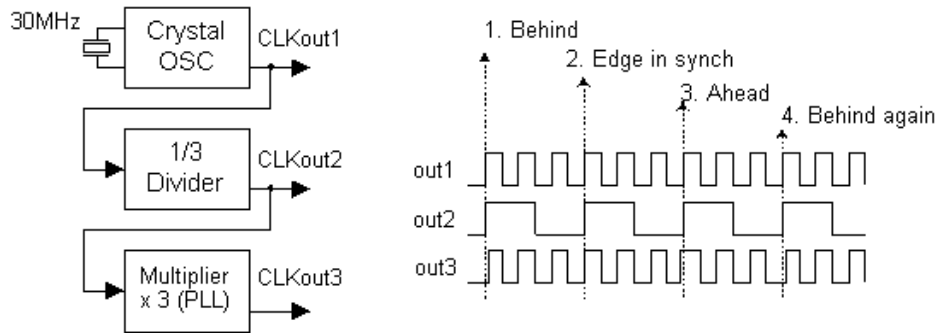


Fig.6: Synchronising the signal.

The new XC25BS3 has an operating voltage range of 3.0 to 5.0V, an operating temperature range of -30 to +80°C, and a power dissipation of 150mW. Supplied in a space-saving microminiature SOT-26 package, the new extremely cost-effective XC25BS3 gives designers significantly more freedom in clock design. Although initially conceived for portable equipment applications, the new PLL IC will prove extremely useful for any design that has a crystal requirement.