

XC612 Series 2 Channel Voltage Detectors

Application Notes

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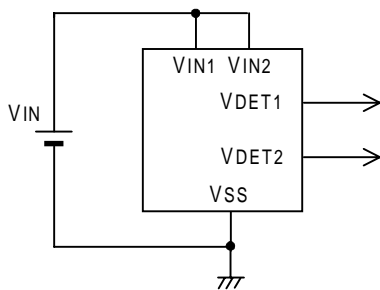
○ Introduction

The XC612 series are highly accurate, low power consumption 2 channel voltage detectors manufactured using laser trimming and CMOS process technologies. The series consists of an output driver circuit, a hysteresis circuit, 2 comparators and a highly accurate standard voltage supply. Detect voltage range is selectable in 0.1V steps from 1.5V to 5.0V. The input (VIN1) for voltage detector 1 (VD1) dually functions as the power supply pin for both detector 1 and detector 2 (VD2).

All the above functions are provided in a super mini-mold SOT-25 package that supports high density mounting.

Voltages higher than 5.0V can be detected by connecting a divided resistor to voltage detector 2 (please refer to the application circuit on p5).

○ Standard Circuits



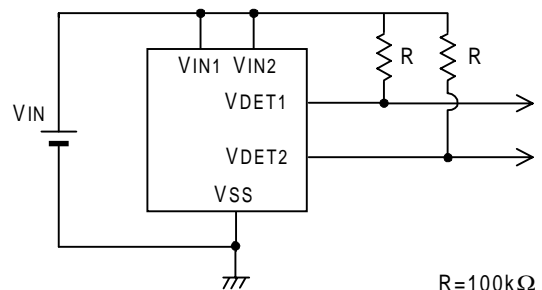
CMOS

CMOS Output Configuration

(under development)

VD1 = CMOS output

VD2 = CMOS output

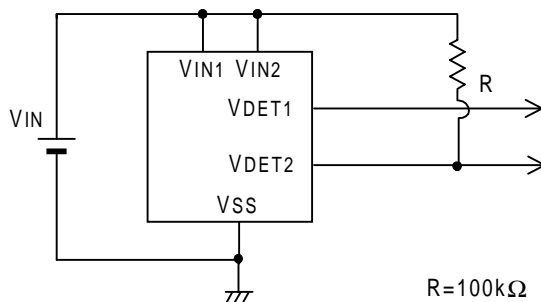


Nch Open Drain

Nch Open Drain Output Configuration

VD1 = Nch open drain output

VD2 = Nch open drain output



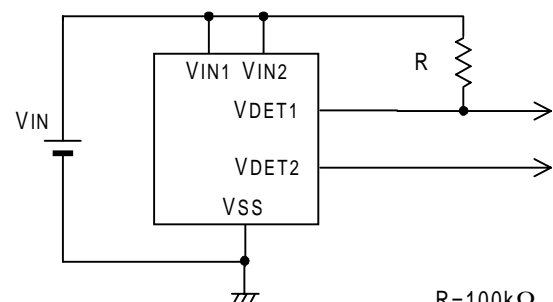
CMOS

Nch Open Drain Output Configuration

(under development)

VD1 = CMOS output

VD2 = Nch open drain output



Nch Open Drain

CMOS Output Configuration

(under development)

VD1 = Nch open drain output

VD2 = CMOS output

Note :

With CMOS output configurations, output voltage (during release), will be equal to input voltage VIN1 (power supply voltage).

○ Notes on Use

1. Absolute Maximum Ratings for the VIN2 Pin

Please note that the absolute maximum rating for the VIN2 pin is $V_{SS} - 0.3V$ to $V_{IN1} + 0.3V$. Please do not exceed this rating.

N.B.

The VIN1 pin dually functions as the IC's power supply and a diode [D] from voltage detector 2's input VIN2 to voltage detector 1's input VIN1 (power supply pin VDD) has been added to protect against ESD. (see diagram below)

Therefore, should VIN2 voltage exceed VIN1 (VDD) voltage, current will flow towards the VIN1 side via the diode.

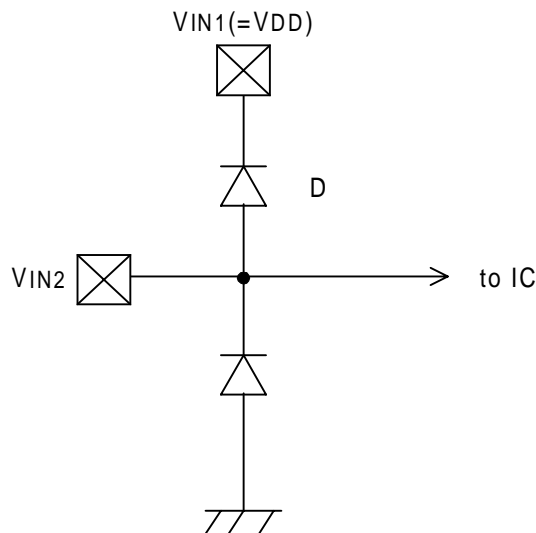


Diagram. VIN2 – VIN1 pin input protection circuit

2. Oscillation (VD1)

Please note that if a resistor is added between the VIN pin and the input with CMOS output configurations, oscillation may occur as a result of load current (I_{OUT}) so please do not use in applications which are fitted with RIN. It should be noted that oscillation may also occur as a result of through current during release with such a set up with CMOS output configurations (irrespective of N-channel output configurations).

However, with a 2 channel voltage detector the only issue concerning oscillation as a result of input resistance relates to the dually functioning VIN1/power supply pin. VIN2 has split resistors so it is possible to divide voltage due to the external resistor (please refer to the application circuits on the following pages).

Please be aware of shifts in detect voltage and release voltage in such cases as such shifts may be brought about by current (V_{IN2} input current) flowing through the IC's internal resistor ($1.1M\Omega \sim 9.3M\Omega$).

3. CMOS Output Configuration (under development)

With CMOS output configurations (under development), output voltage (during release), will be equal to input voltage VIN1 (power supply voltage).

4. Operational errors resulting from steep frequency inputs

Should steep start up voltages be input at the VIN pin, frequencies output from VOUT may become distorted so please regulate input frequency start up time (MIN) to a standard of more than 5 μ seconds/V.

5. Pull up Resistance with Nch Open Drain Configurations

If the pull up resistance value is extremely large with Nch open drain output configurations, output voltage may drop during release operations as a result of the N-channel transistor leak current within the IC.

It is therefore recommended that a pull up resistance of less than 470k Ω be used.
(a pull up resistor is not necessary with CMOS output configurations)

○ Application Circuits

1. High Voltage Detection Circuit

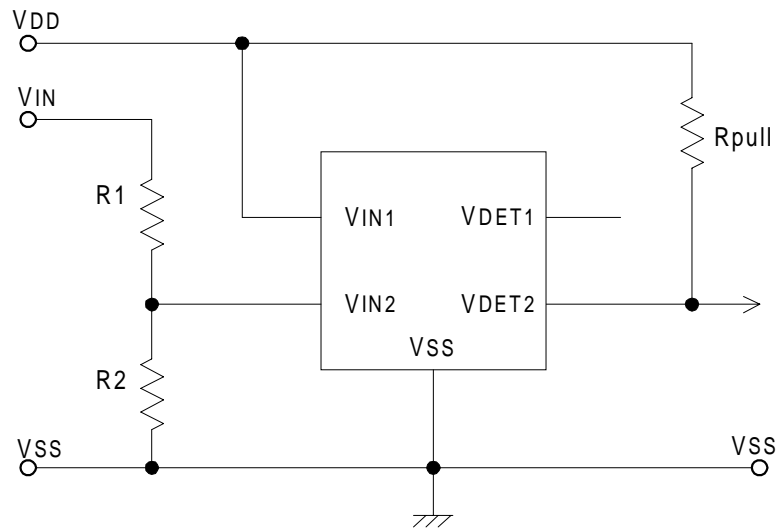


Diagram. High Voltage Detect Circuit

XC612 series (VD2 can also be used for CMOS output configurations)

Peripherals :

R1 : 20k Ω

R2 : 10k Ω

Ex.) Detect voltage VDF2 = 3.0V

Set-up detect voltage VDH2 = 9.0V

Hysteresis range increases from 0.15V(typ) to 0.45V
(Please refer to the notes on detect voltage VDH2 and
hysteresis range VHYSH2 provided below)

Rpull : 100k Ω

Notes :

The value for detect voltage VDH2 and hysteresis range VHYSH2 can be calculated as follows :

$$VDH2 = VDF2 \cdot (R1 + R2) \div R2 \quad (V)$$

$$VHYSH2 = VHYS2 \cdot (R1 + R2) \div R2 \quad (V)$$

where VDF2 = the IC's detect voltage value

VDH2 = the actual circuit's detect voltage value

VHYS2 = the IC's hysteresis range

VHYSH2 = the actual circuit's hysteresis range

(1) Please be aware that V_{HYSH2} and V_{DH2} will be higher than the calculated values due to V_{IN2} input current. With resistance values for R_1 and R_2 below $47k\Omega$, the voltage accuracy of the single IC unit's detect voltage value will be more than 2%.

(2) Please ensure that the V_{IN2} pin's input voltage is lower than $V_{IN1} + 0.3V$.

N.B. :

Should your required voltage detection level be outside the ranges stated herein, it is possible to achieve a V_{D2} detect voltage higher than the IC's established values by using divided resistors.

2. A circuit that will allow you to check which of the 2 voltage detectors carried out detection functions

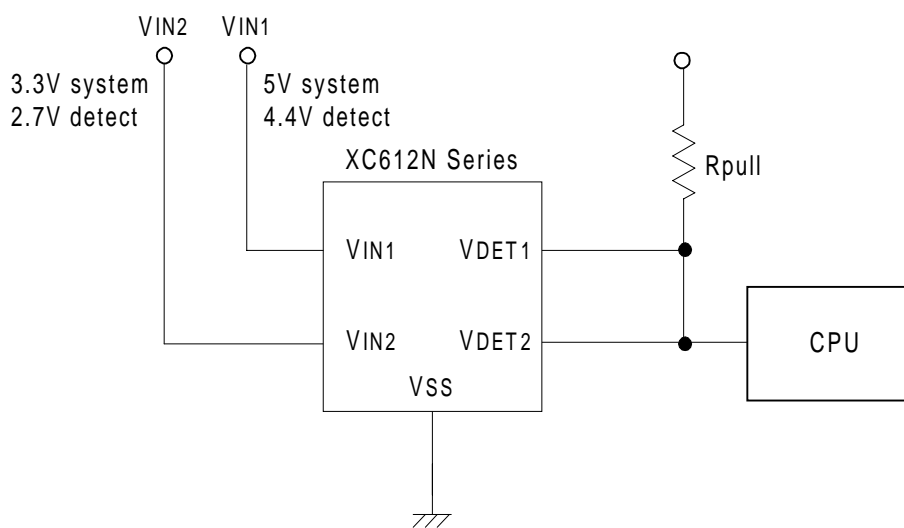


Diagram. How to discover which voltage detector detected !

XC612 series (Nch open drain output type)

Peripherals :

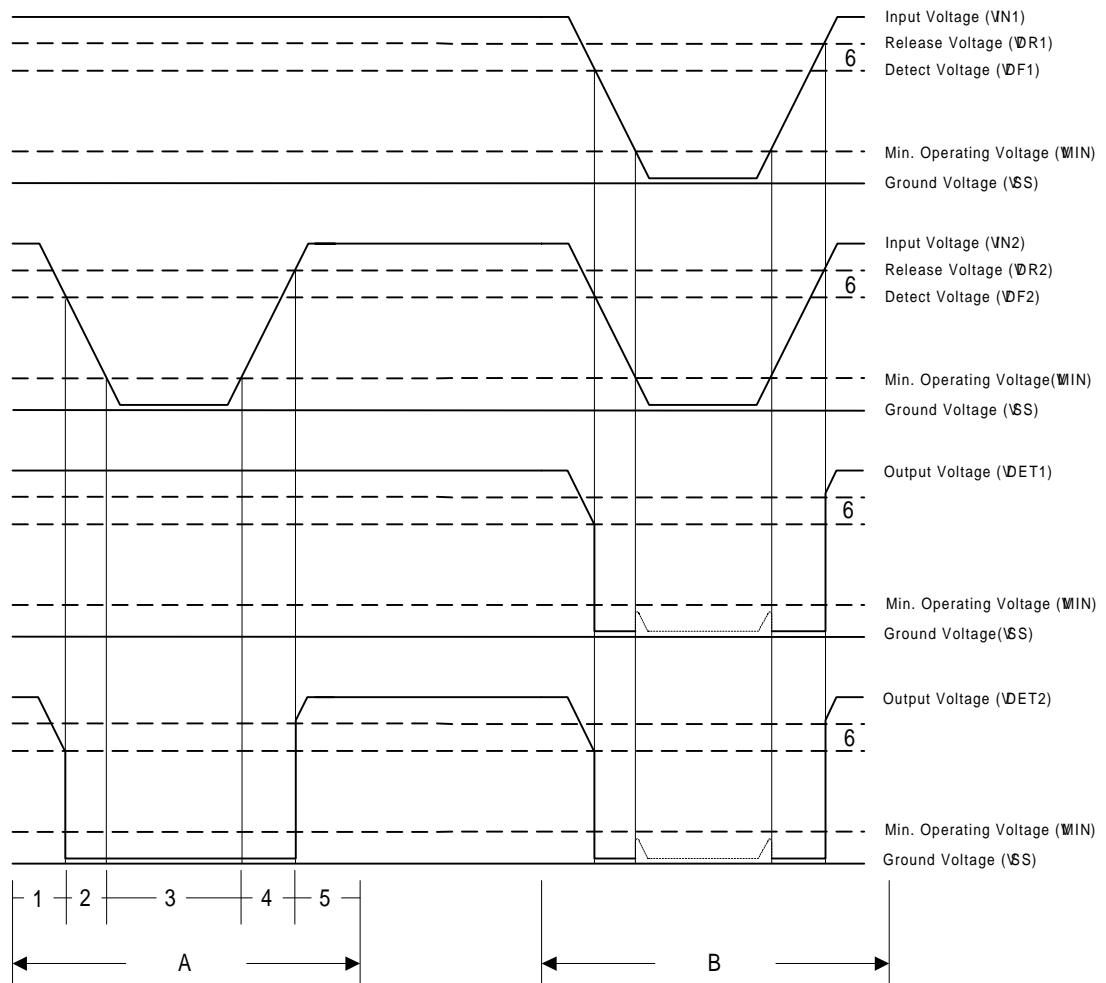
R_{pull} : $100k\Omega$

N.B.

By using only 1 resistor and 1 input on the CPU side it is possible to find out which of the 2 systems ($V_{D1}=5V$; $V_{D2}=3.3V$) carried out detect functions.

○ Appendix

Time Chart



Functional Explanation (both channels as Nch open drain outputs)

Timing Chart A (VIN1 : more than release voltage, VIN2 : sweep voltage)

Because a voltage higher than the lowest functional voltage is applied to the voltage input pin (VIN1), ground voltage level will be output at the output pin (VDET2) during stage 3. (Stages 1,2 4 & 5 will follow the conditions of B).

Timing Chart B (VIN1 = VIN2)

1. Should a voltage higher than the release voltage (VDR) be applied at the power supply pin (VIN1, VIN2), input voltage (VIN1, VIN2) will gradually decrease. Should a voltage higher than the detect voltage (VDF) be applied at the power supply pin (VIN1, VIN2), a condition of high impedance will exist at the output pin (VDET1, VDET2). Note that the voltage will be pulled up voltage should the pin be pulled up.

With CMOS output configurations (under development), output voltage will become input voltage VIN1 (power supply voltage).

2. When input voltage (V_{IN1}, V_{IN2}) falls below detect voltage (V_{DF}), output voltage (V_{DET1}, V_{DET2}) will equal ground voltage (V_{SS}).
3. When V_{IN1}, V_{IN2} falls to a level below that of the minimum operating voltage (V_{MIN}), output becomes unstable.
However, should input voltage (V_{IN2}) fall below V_{MIN} , ground voltage (V_{SS}) will be output at the output pin (V_{DET2}) if the power supply (V_{IN1}) is within the functional voltage range.
Generally, output will be equal to the pull up voltage because the output is pulled up.
4. When V_{IN1}, V_{IN2} rises above the V_{SS} level (excluding the area lower than min. operating voltage), output voltage (V_{DET1}, V_{DET2}) will remain equal to ground level voltage until the release voltage level (V_{DR}) is reached.
5. Voltage at the output pin (V_{DET1}, V_{DET2}) will come to rely upon pull up due to input voltage (V_{IN1}, V_{IN2}) exceeding release voltage (V_{DR}).

Note : The difference between V_{DR} and V_{DF} ('6') represents the hysteresis range.